Processor Power Controller with Intel VR9, VR10, and AMD Hammer VID Support (ISL6563EVAL1)

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Author: Bogdan M. Duduman

Introduction

The progress of the advanced computing cores coming from microprocessor manufacturers such as Intel and AMD have necessitated a change in the topology of the switching regulators traditionally used to power them. Multiphase buck regulators have proven to be the topology of choice for such high-current applications. The ISL6563 is a cost-effective alternative to a core power solution for a typical VRM9 or VRM10 Pentium, or Hammer-class processor system. Utilizing a proven $r_{DS(ON)}$ sensing 2-phase buck approach, the ISL6563 consists of a multiphase core controller with a selectable VID input and two half-bridge, high current drivers, along with all the necessary protection and coordination features required by a typical VR9, VR10, or AMD Hammer design.

The ISL6563EVAL1 evaluation board embodies a 55-60A regulator solution targeted at supplying power to the core of either of the three types of processors mentioned above. The physical board ships out configured for VR10 VID coding, but can be easily modified to support any of the other two VID tables.

Quick Start Evaluation

To facilitate the evaluation of the ISL6563 in a typical setting, the ISL6563EVAL1 is designed to be powered primarily from an ATX supply. However, the board does have terminals that allow it to be powered from standard laboratory power supplies. Figure 1 details the available input and output connections.

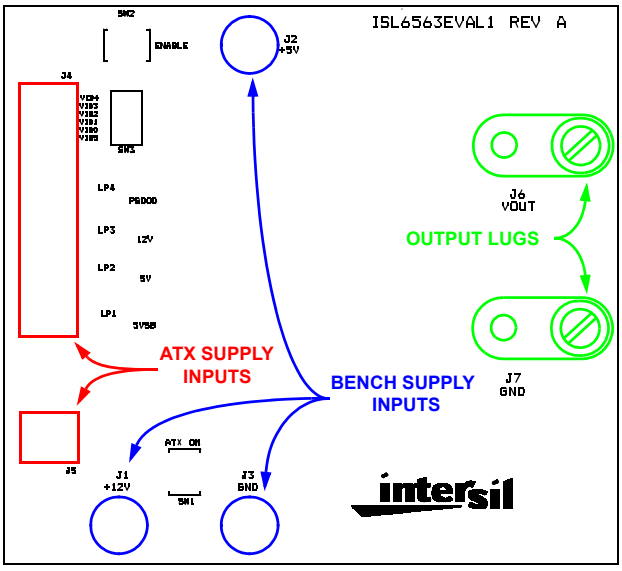

FIGURE 1. ISL6563EVAL1 INPUT AND OUTPUT CONNECTIONS

Circuit Setup

Before connecting an input supply to the board, consult and familiarize yourself with the circuit schematic and the connection options offered by the ISL6563EVAL1.

- **Set Switches**

Ensure the 'ATX ON' (**SW1**) and 'ENABLE' (**SW2**) switches are in the off position (away from 'ATX ON' and 'ENABLE' markings, respectively).

SW3 selects the output voltage setting and DAC compatibility (Intel VRM9.0, or AMD Hammer; when not in VRM10 setting). Please consult the ISL6563 datasheet and the circuit schematic for a thorough understanding of the available options for setting the output voltage. Figure 2 details the typical default configuration for SW3 when the board is received. In this default setting, the evaluation board is set for VRM10 support; all sections of SW3 representing inputs into the 6-bit VID DAC.

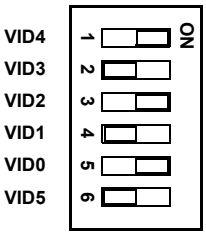

FIGURE 2. TYPICAL SW3 DEFAULT SETTING (1.600V; VRM10)

- **Set DAC Compatibility (optional)**

Should the default VRM10.0 DAC compatibility not be the desired version, VRM9.0 or AMD Hammer DAC compatibility can be programmed by removing R22 (see evaluation board schematic). Once the $\overline{\text{VRM10}}$ pin is open, the VID5 section of the SW3 switch selects the new DAC compatibility: set to the ON position for AMD Hammer or leave in the OFF position for VRM9.0 compatibility. Consult the ISL6563 datasheet for more information.

- **Hookup Guide Using a Standard ATX12V Supply**

Connect the 20-pin main and the 4-pin 12V ATX connectors to the J4 and J5 mating on-board connectors. Connect an output load to the evaluation board's output (VOUT and GND; J6 and J7); an electronic load is generally recommended for its ease of use.

- **Hookup Guide Using Standard Bench Supplies**

Connect a 5V, 1A supply to the +5V input (J2) and a 12V, 12A, supply to the +12V input (J1); connect both ground leads to the GND (J3) input. Connect an output load to the evaluation board's output (VOUT and GND; J6 and J7); an electronic load is generally recommended for its ease of use.

Operation

- **Provide Power to the Board**

If using an ATX supply, plug it into the mains, and, if the supply has an AC switch, turn it on. The '5VSB' LED should light up, indicating the presence of 5V standby. Flip on the 'ATX ON' switch; immediately thereafter, the '5V' and '12V' LEDs should light up indicating the presence of main ATX 5V and 12V on the evaluation board.

Should bench supplies be used, simply turn them on; any turn-on sequence is fine. The '5V' and '12V' LEDs should light up, but in this case, the '5VSB' LED should stay off (there is no 5V standby voltage provided by bench supplies).

To enable the circuit for operation, flip on the 'ENABLE' switch (SW2); the circuit should immediately bring up the output voltage corresponding to the DAC setting.

- **Examine Start-Up Waveforms/Output Quality Under Varying Loads**

Start-up is immediate following application of bias voltage. Using an oscilloscope or other laboratory equipment, you may study the ramp-up and/or regulation of the output voltage. Loading of the output can be most easily done via an electronic load; however, most any other method will work as well.

- **Examine VID-Directed Output Voltage Transitions (VRM9.0 or AMD Hammer DAC Settings Only)**

Although the evaluation board ships populated for VRM10 DAC compatibility, depopulating R22 changes the DAC compatibility to either VRM9.0 or AMD Hammer (check circuit schematic and ISL6563 datasheet).

In either of these DAC compatibility modes, the VID setting can be changed while the board is enabled and operational, resulting in an immediate and controlled change in the output voltage setting as per the new VID code selected. Exercise this function and observe the resulting changes under desired loading conditions.

Fault Handling

The ISL6563 protects the output against over-current (OC) and over-voltage (OV) events.

In case of an over-current event, the circuit turns off and attempts an output soft-start (SS) after waiting for a time period equaling two SS cycles. In the unlikely case of an over-voltage event, the controller turns on the lower MOSFETs as needed in order to lower the output voltage below the falling OV threshold. However, the OV behavior is masked by the normal feedback loop behavior; as soon as the output starts to exceed the internal reference the lower MOSFETs' duty cycle is increased as necessary to maintain the output regulation.

The behavior of the circuit, in either situation (OC or OV), repeats until the fault condition is removed or the circuit is disabled. Review the appropriate datasheet sections for more details.

Reference Design

General

The evaluation board is built on 2-ounce, 4-layer, printed circuit board (see last three pages of this application note for layout plots). The board is designed to support a continuous output current level of up to 55-60A, while operating at room temperature, under natural convection cooling; consult the 'Modifications' section for information on modifying the evaluation board to meet your special needs.

Performance

Figures 3 through 11 depict the evaluation board's performance during typical operational situations.

Soft-Start Start-Up

Figure 3 details a typical ISL6563EVAL1 start-up. For this scope capture, the ATX supply powering the board is turned on via SW1 prior to time T0. At time T0, SW2 is enabling the circuit for operation and EN pin starts to rise. As the EN pin is surpassing its threshold at time T1, a soft-start sequence is initiated and the output voltage is increased, under a constant rate of rise, to its set value. Once the output voltage

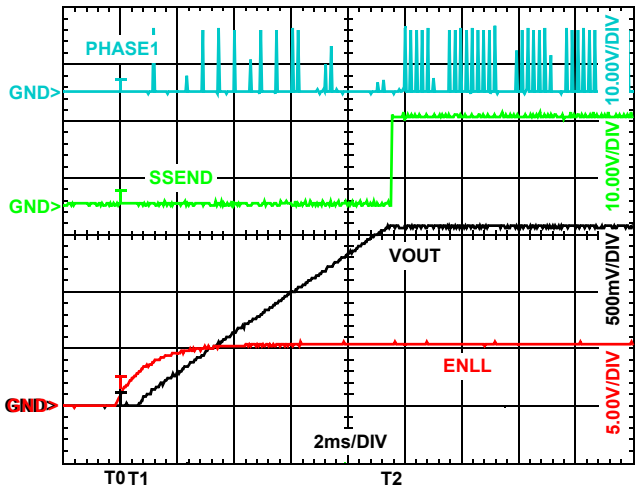

FIGURE 3. ISL6563EVAL1 NORMAL START-UP (V_{DAC} = 1.600V)

rises up to its set point, SSEND (Soft-Start END) pin is released (T2), signaling the conclusion of the start-up sequence.

Special consideration is given to start-up into a pre-charged output (where the output is not 0V at the time the SS cycle is initiated). Under such circumstances, the ISL6563 keeps off both sets of output MOSFETs until the internal ramp starts to exceed the output voltage sensed at the FB pin. This special scenario is detailed in Figure 4. The circuit is enabled, similar to Figure 3, at time T0. As the internal ramp exceeds the magnitude of the output voltage at time T1, the

MOSFETs drivers are enabled and the output voltage ramps up in a seamless fashion from the pre-existent level to the DAC-set level, reached at time T2.

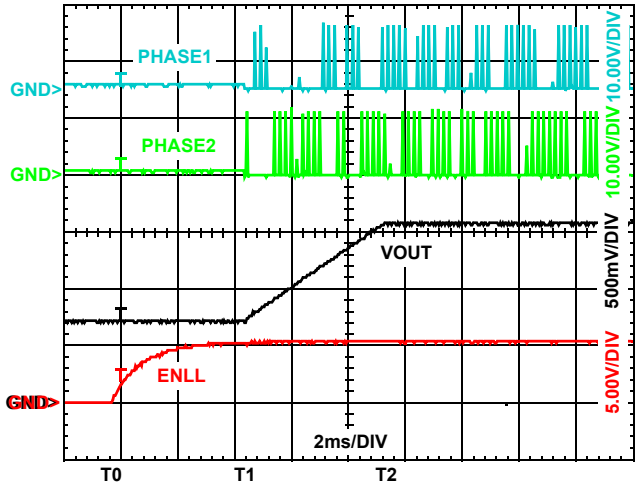

FIGURE 4. ISL6563EVAL1 START-UP INTO A PARTIALLY CHARGED OUTPUT (V_{DAC} = 1.600V)

A second scenario can be encountered with a pre-charged output: output being pre-charged above the DAC-set point, as shown in Figure 5. In this situation, the ISL6563 behaves in a way similar to that of Figure 4, keeping the MOSFETs off until the end of the SS ramp. However, once the end of the ramp has been reached, at time T1, the output drives are enabled for operation, and the output is quickly drained down to set-point level.

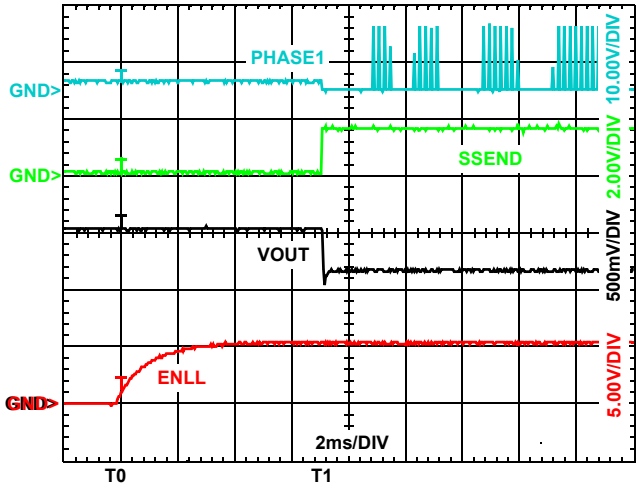

FIGURE 5. ISL6563EVAL1 START-UP INTO AN OVER-CHARGED OUTPUT (V_{DAC} = 1.200V)

An OV condition during start-up will take precedence over this normal start-up behavior, but will allow reversal back to normal behavior as soon as the condition is removed or brought under control.

Over-Current Response

Figure 6 displays a pattern of typical circuit behavior when encountering an OC situation. At time T0 an output short-circuit is applied, resulting in the circuit shutting down immediately and initiating a wait period of two SS cycles, T0 to T1. As the wait period ends at time T1, the circuit initiates a new SS cycle, attempting to bring the output back within regulation limits. As the output voltage increases and the output short-circuit increases, the OC limit is reached, again, at time T2, causing the circuit to repeat the shut-down and wait cycle. Should the short-circuit have been removed prior to time T2, the circuit would have brought the output in regulation and continued operating as it did prior to the fault condition being applied.

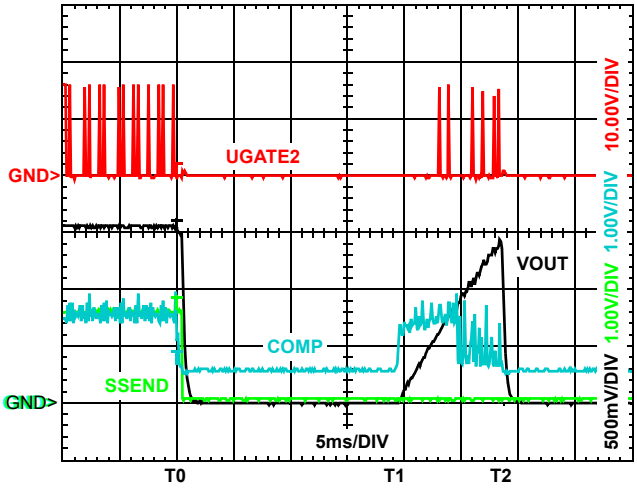

FIGURE 6. ISL6563EVAL1 OVER-CURRENT PROTECTION

Pre-POR Over-Voltage Protection

Typically, complex integrated circuits (including power management controllers) are internally disabled, and various internal circuitry is reset as soon as there is sufficient bias voltage for this task to be achieved. This procedure is necessary to insure that the various internal circuits are always starting from known states, and also to insure they are not enabled until they have sufficiently high bias to ensure behavior consistent with their designed functions.

Concerns have been voiced over situations where, due to manufacturing defects, process variations, or other factors, the upper MOSFET could emerge shorted from the assembly operations. Given the fact the controller is not enabled for operation until the bias voltage reaches roughly 90% of its final value, and given the typical ATX supply architecture coupling the 5V and 12V on the same HF transformer (outputs thus become ratiometrically coupled), a shorted upper MOSFET could cause the output of the circuit to ramp up to about 10.8V before the controller can detect and take action against the over-voltage condition.

The pre-POR OV protection cleverly attempts to limit the rise of the output voltage in such a scenario to the lowest level possible in the given application circuit: the $V_{GS(TH)}$ of the lower MOSFETs. This feat is achieved via a special circuitry acting upon the lower MOSFETs' gates while the ISL6563's VCC level is below POR threshold, by effectively shorting the gates to the drains of the respective MOSFETs via finite impedances (LGATE to PHASE; typically 5kΩ).

Figure 7 details the typical circuit behavior when this feature is activated. A very small impedance was placed across Q1 in order to simulate a manufacturing short-circuit, then the ATX supply was enabled, at time T0. At time T1, the 5V and 12V outputs of the ATX supply begin to ramp up, and, with the 12V, so does the output of the circuit. Since the output inductors do not carry any significant current, the PHASE node follows the output voltage closely and so does LGATE1 (LGATE2, not shown, exhibits identical behavior). The moment LGATE pins reach the $V_{GS(TH)}$ of the lower MOSFETs, at time T2, the rise of the output voltage is quickly curbed.

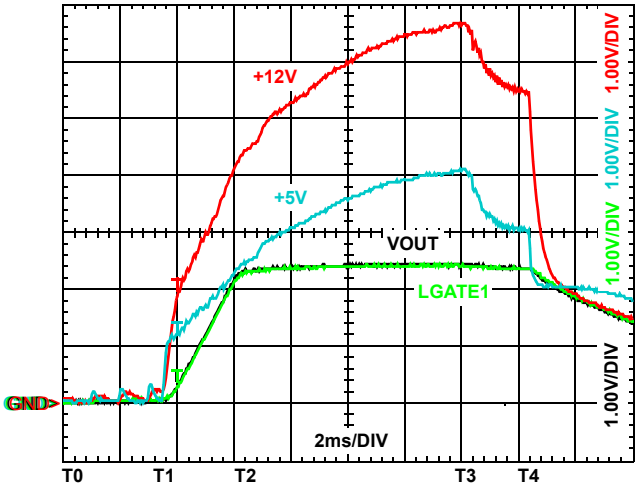

FIGURE 7. ISL6563EVAL1 PRE-POR OUTPUT OVER-VOLTAGE PROTECTION (START-UP WITH SHORTED Q5)

Even though the output voltage no longer increases, the current sunk from the ATX input supply is increasing from T2 to T3, causing the supply to reach its OC threshold and trip. At time T4, the current sunk from the input supply diminishes and the 12V input collapses to the V_{OUT} level (a small constant-current output load discharges the output from that point on).

Normal Over-Voltage Protection

While biased and operational, the ISL6563 benefits from a secondary over-voltage protection. Normally, the feedback loop takes control and prevents the OV condition before the real OVP mechanism can begin operation; both activating the lower MOSFETs, it is hard to distinguish between the two.

Figure 8 details the operation of the OVP mechanism while the ISL6563 is fully biased and the circuit is operational. At time T0 Q1 is shorted, and as a result, the increase in the output voltage makes the controller decrease the duty cycle. Turning on the lower MOSFET, while the upper is shorted, results in a very large current being drawn from the input supply, further leading to the effective collapse of the +12V input. Following, at time T1, the ATX supply's OC protection kicks in; the lack of current being delivered from the input is causing the output to ramp down below the regulation setpoint, from T1 to T2. At time T2, the +5V input drops below the falling POR threshold of the ISL6563, and the controller stops operating. Due to the short still present across Q1, the output voltage drifts slightly higher to the potential still held in the input supply's output capacitors.

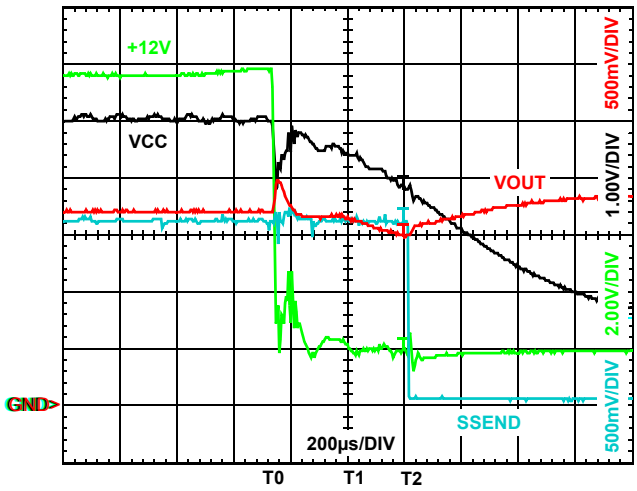

FIGURE 8. ISL6563EVAL1 OUTPUT OVER-VOLTAGE PROTECTION

Should strict OVP thresholds need be monitored at all times, it is recommended the ISL6563 bias is provided from a source which is always present (independent of the power conversion input); in a computer system, the source that could be used is the +5VSB. On the evaluation board, this can be achieved by depopulating R7 and using the same resistor to populate R9.

Output Transient Response

The ISL6563EVAL1 circuit is designed to exhibit output voltage droop, at a slope of roughly 1mΩ. Figure 9 details the circuit's response to a load step transient. During the T0-T1 transient duration, the output voltage droops, corresponding to the load slope programmed. Although the droop cannot be eliminated completely, it can be easily reduced to relatively small magnitudes. However, in most instances, the presence of some amount of output droop helps minimize the total

peak-to-peak output excursion when responding to fast transient loading.

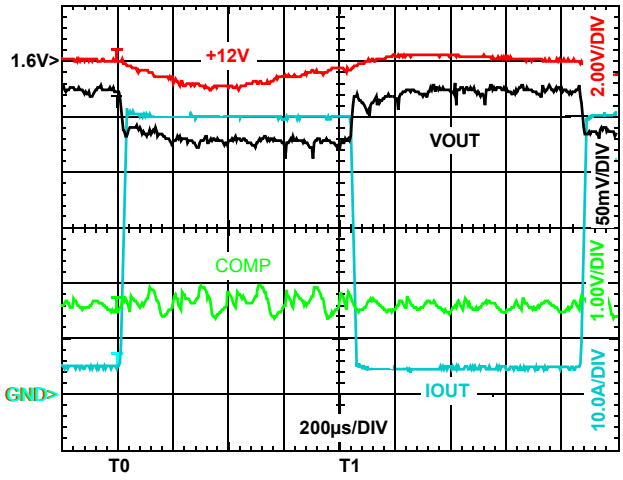

FIGURE 9. ISL6563EVAL1 LOAD TRANSIENT RESPONSE

Channel-to-Channel Current Sharing

Channel-to-channel current sharing is an important feature of a multi-phase controller, helping ensure uniform thermal performance across the individual power trains. Figure 10 details the current sharing during transient response, offering a glimpse into the tight channel-to-channel current balancing during both steady-state, as well as during dynamic response operation.

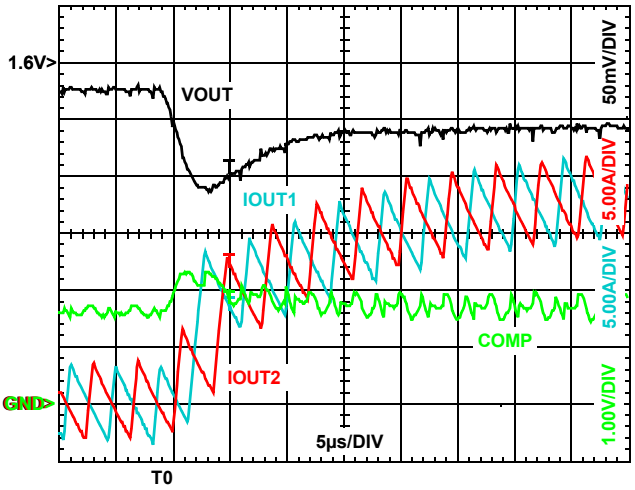

FIGURE 10. ISL6563EVAL1 PHASE-TO-PHASE CURRENT SHARING

Channel-to-channel current sharing/balancing is influenced primarily by the lower MOSFETs' $r_{DS(ON)}$ matching and the layout parasitics. As the ISL6563 does not provide any means of adjusting the channel-to-channel current sharing, close attention should be paid to these design parameters.

Switching Efficiency

Figure 11 highlights the evaluation board's conversion efficiency, including all bias power. The measurements were performed with all board components at (or very close to) room temperature.

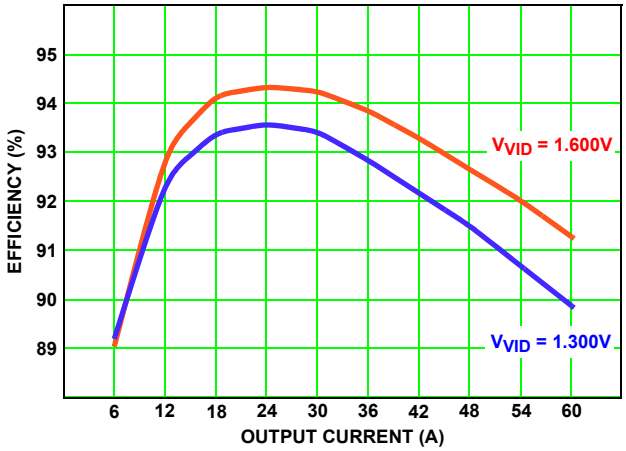

FIGURE 11. ISL6563EVAL1 MEASURED EFFICIENCY

Modifications

Adjusting the Output Voltage

The output voltage can be adjusted via the DAC-set internal reference. Please consult the datasheet for the available voltage ranges and the required settings.

The offset pin (OFS) allows for small-range (less than 100mV), positive or negative, offsetting of the output voltage. Should an output voltage setting outside the normal range provided via the internal DAC be required, a separate resistor from FB to GND or to VCC will be required in order to increase or decrease, respectively, the output voltage.

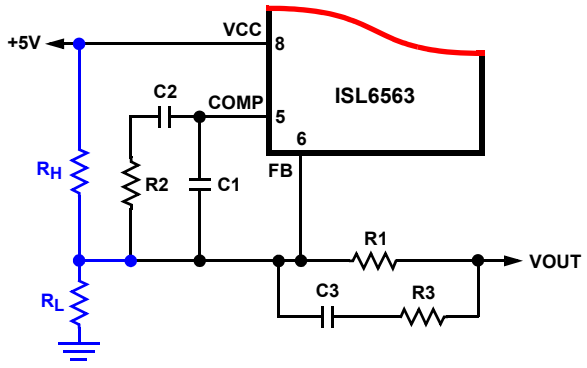

FIGURE 12. ADJUSTING V_{OUT} OUTSIDE THE DAC RANGE

Figure 12 details the connection of such a resistor in the ISL6563-based circuit. R_H would be used should a lower output voltage be desired, while R_L would be used in case of

a higher voltage. Assuming the OFS pin is left floating in such a situation (no offset programmed), use the following relationships to compute the value of either resistor based on the known parameters.

$$R_H = \frac{R1 \cdot (V_{VCC} - V_{DAC})}{V_{DAC} - V_{OUT}}$$

$$R_L = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

Down-Converting From a Different Input Voltage

The ISL6563EVAL1 is primarily set up to use an ATX computer supply as a bias and down-conversion source. However, when powered from bench supplies, the down-conversion input labeled '+12V' can be adjusted down as desired. If experimenting with a lower voltage, be mindful of a few aspects:

- The duty cycle of the controller is limited to 66%; the circuit will not be capable of properly regulating the output voltage should the input be reduced to a level low enough to induce duty cycle saturation
- The input-RMS current will likely increase as the input voltage is decreased; maximum will be achieved at duty cycles around 25% to 35%
- As the evaluation board (as shipped) was not optimized for high duty cycle operation, closely monitor the board temperatures and increase the output current only as allowed by the board thermal situation
- The reduced input voltage will decrease the amount of loop gain the modulator provides in the feedback loop, as a result, expect a more sluggish transient response when operating the board at reduced down-conversion voltage

Conclusion

The ISL6563EVAL1 evaluation board showcases a highly integrated approach to providing control in a variety of applications, with emphasis on computer systems. The sophisticated feature set and high-current MOSFET drivers of the ISL6563 yield a highly efficient power conversion solution with a reduced number of external components in a compact footprint.

References

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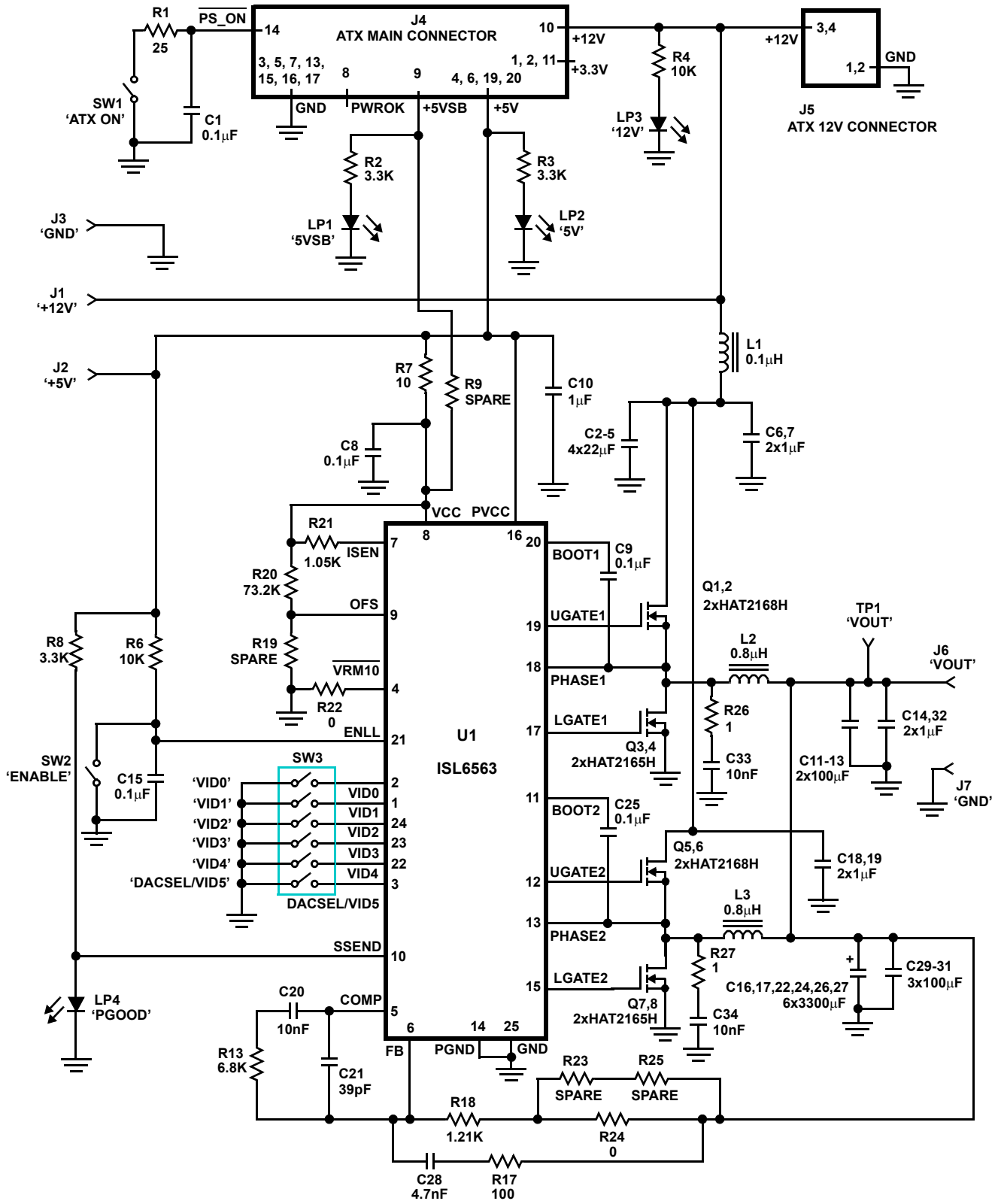
ISL6563EVAL1 Schematic

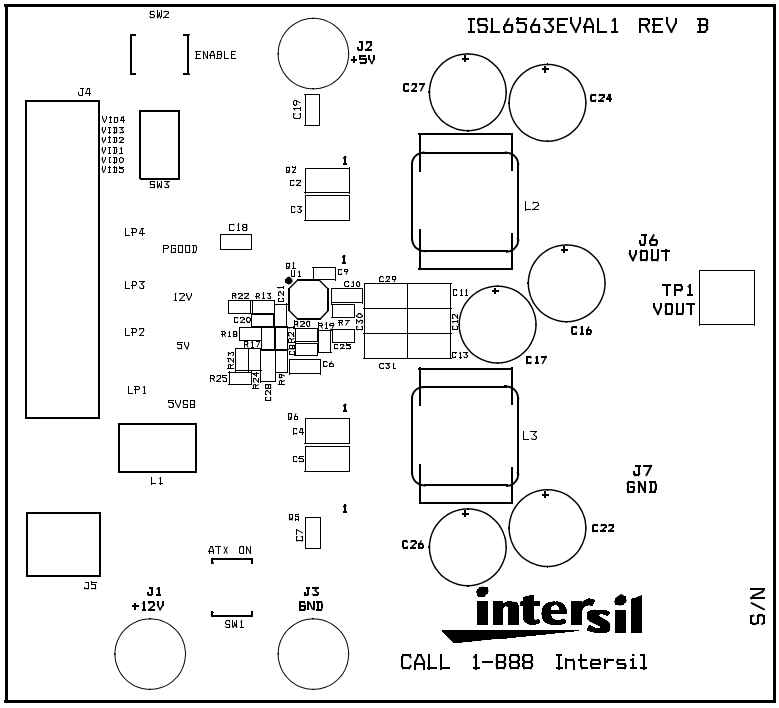


Bill of Materials for ISL6563EVAL1

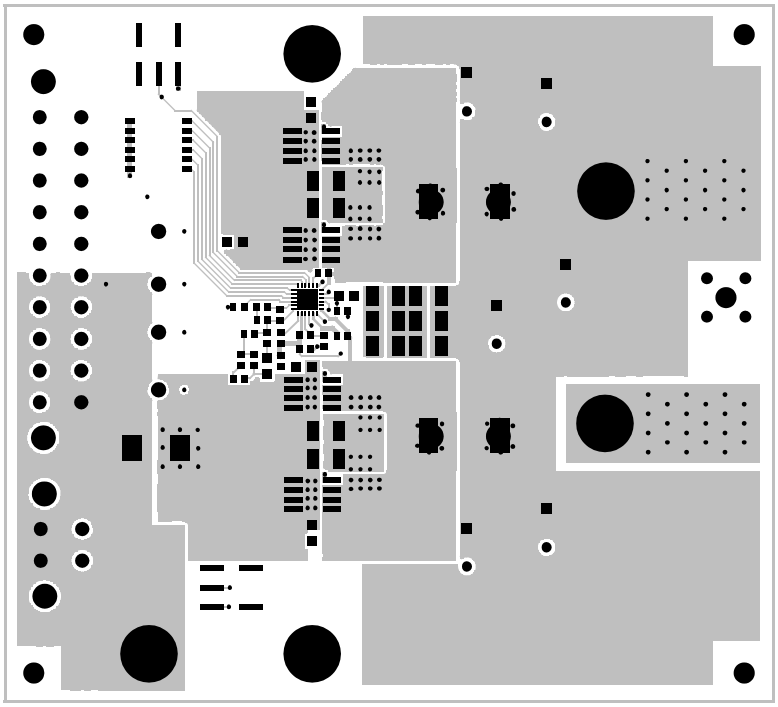
REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE/ FOOTPRINT	MANUF. OR VENDOR	QTY
C1, 8, 9, 15, 25	0.1μF Ceramic	Ceramic Capacitor, X7R, 25V	0603	Any	5
C2-5	C3225Y5V1C226Z	Ceramic Capacitor, Y5V, 16V	1210	TDK	4
C6, 7, 10, 14, 18, 19, 32	1μF Ceramic	Ceramic Capacitor, X7R, 16V	0805	Any	7
C11, 13, 29-31	C3225X5R0J107M	Ceramic Capacitor, X5R, 6.3V	1210	TDK	5
C16, 17, 22, 24, 26, 27	6.3MBZ3300M	Al. Electrolytic Capacitor, 6.3V, 3300μF	10 x 23	Rubycon	6
C20, 33, 34	10nF Ceramic	Ceramic Capacitor, X7R, 25V	0603	Any	3
C21	39pF Ceramic	Ceramic Capacitor, X7R, 50V	0603	Any	1
C28	4.7nF Ceramic	Ceramic Capacitor, X7R, 25V	0805	Any	1
C12	spare				
J1,2	111-0702-001	Banana Jack/Binding Post, Red		Digikey	2
J3	111-0703-001	Banana Jack/Binding Post, Black		Digikey	1
J4	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		Molex	1
J5	39-29-9022	4-pin Mini-Fit, Jr.™ Header Connector		Molex	1
J6, 7	KPA8CTP	Tin-Plated Lug Terminal		Burndy	2
L1	P1681	0.1μH inductor, SM Inductor	8 x 15	Pulse	1
L2, 3	PG0077.801	0.8μH inductor, SM Inductor	10 x 17	Pulse	2
LP1-4	L63111CT-ND	Miniature LED, through-board indicator		Digikey	4
Q1, 2, 5, 6	HAT2168H	MOSFET, 30V, 8.8mΩ	LFPAK	Renesas	4
Q3, 4, 7, 8	HAT2165H	MOSFET, 30V, 3.4mΩ	LFPAK	Renesas	4
R1	24Ω	Resistor, 5%, 0.1W	0603	Any	1
R2, 3, 8	3.3kΩ	Resistor, 5%, 0.1W	0603	Any	3
R4, 6	10kΩ	Resistor, 5%, 0.1W	0603	Any	2
R7	10Ω	Resistor, 5%, 0.1W	0603	Any	1
R22, 24	0Ω	Shorting resistor	0603	Any	2
R26, 27	1Ω	Resistor, 5%, 0.16W	0805	Any	2
R20	73.2kΩ	Resistor, 1%, 0.1W	0603	Any	1
R21	1.05kΩ	Resistor, 1%, 0.1W	0603	Any	1
R18	1.21kΩ	Resistor, 1%, 0.1W	0603	Any	1
R17	100Ω	Resistor, 5%, 0.1W	0603	Any	1
R13	6.8kΩ	Resistor, 5%, 0.1W	0603	Any	1
R9, 19, 23, 25	spare				
SW1, 2	GT11MSCKE	Miniature Switch, Single Pole, Double Throw		C&K	2
SW3	TDA06H0SK1R	Miniature Switch, SPST, 6 positions		C&K	1
TP1	131-5031-00	Board Test Point (bag of 25)		Tektronix	1/25
	0293-0-15-01-16-01-10-0	Socket		Mill-Max	1
U1	ISL6563CR	Two-Phase Multiphase PWM Buck Controller with Integrated MOSFET Drivers	QFN-24	Intersil	1
	SJ5003-0-ND	3M rubber bumper		Digikey	6

ISL6563EVAL1 Layout

TOP SILK SCREEN

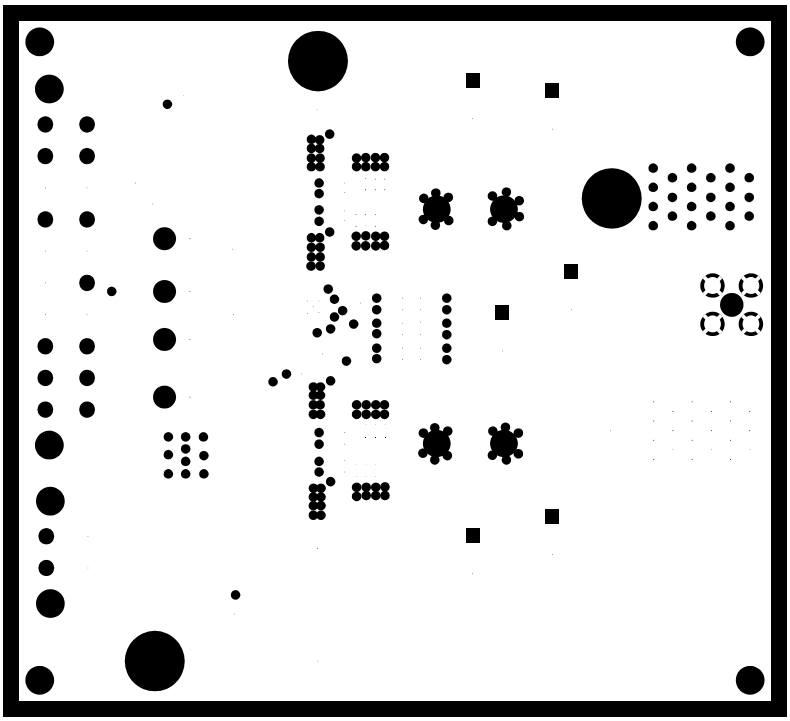


TOP LAYER (1st)

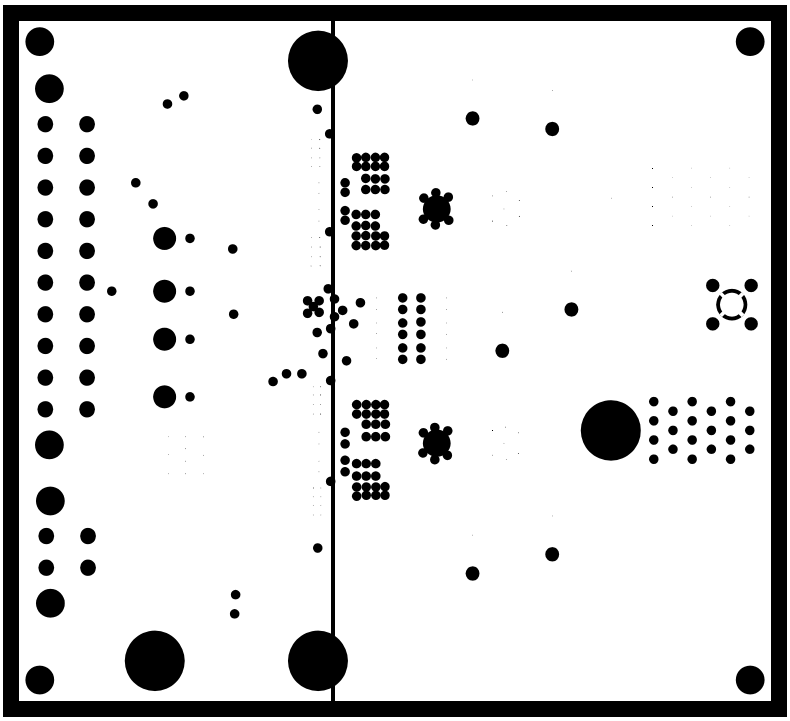


ISL6563EVAL1 Layout (Continued)

GROUND LAYER (2nd)

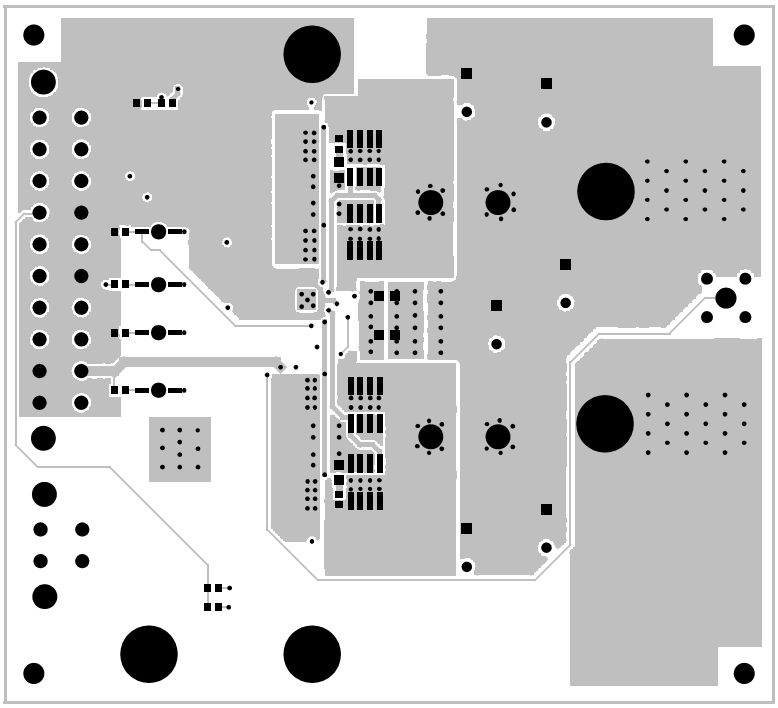


POWER LAYER (3rd)



ISL6563EVAL1 Layout (Continued)

BOTTOM LAYER (4th)



BOTTOM SILK SCREEN